sensor, for maintaining an accumulated charge potential of said sensor at a substantially zero level, and for generating a sensor output current from said detected positive and negative charges;

an integrator supplied with said sensor output current which integrates said sensor output current to produce an integrated signal representing a status of said sensor; and

said integrator including a current-to-frequency converter which converts said sensor output current into a frequency signal having a frequency representing a level of said sensor output current, and a counter supplied with said frequency signal for subjecting said frequency signal to a counting operation to obtain said integrated signal.

15. An apparatus as claimed in claim 14 wherein said sensor is a piezoelectric sensor.

16. An apparatus as claimed in claim 14 wherein said integrator further includes:

a combining unit for combining said sensor output signal with a DC signal, to obtain a combined signal having an offset DC level, said DC signal being such that a change of sign of said sensor output current does

not result in any change of sign of said combined signal, said combine signal being supplied to said current-to-frequency converter, and causing an output from said counter to contain an integration contribution from said DC signal; and

a unit supplied with said output from said counter for removing said integration contribution from said DC signal to produce said integrated signal.

17. An apparatus as claimed in claim 16 wherein said unit for removing said integrated contribution from said DC signal comprises:

a first switching stage for repeatedly switching said sensor output current between two parallel signal processing paths;

in each of said two parallel signal processing paths, a unit for generating a processing path output signal which comprises an information output signal dependent on said combined signal when the signal processing path containing the unit is receiving the sensor output current and which comprises an idle output signal dependent on said DC signal when the signal processing path containing the unit is not receiving the sensor output current; and

a unit which combines the respective output signals from said two parallel signal processing paths.

18. An apparatus as claimed in claim 17 wherein each of said two parallel signal processing paths comprises:

a signal path combiner for combining the sensor output current, when said sensor output current is received in the signal processing path, with said DC signal to obtain a signal path combined signal having said DC offset level; and

a converter for combining the signal path combined signal into a frequency signal having a frequency corresponding to a level of the frequency path combined signal, so that said output signal has a non-zero frequency; and

wherein said unit for combining said output signals from the two parallel signal processing paths is a counter.

19. An apparatus as claimed in claim 16 wherein said integrator further includes:

a first capacitor and a second capacitor;

circuitry supplied with said combined signal for alternatingly charging and discharging said first and second capacitors dependent on said combined signal so that when one of said first and second capacitors as being charged by said combined signal the

other of said first and second capacitors is being discharged, said circuitry causing a completed charging of said first capacitor to initiate discharging of said first capacitor and charging of said second capacitor, and vice versa, and wherein each discharging of each of said first and second capacitors generates a discharge pulse, thereby producing a plurality of discharge pulses; and

a counter supplied with said discharged pulses for counting said discharge pulses and thereby generating a count value representing an integrated signal of said combined signal.

20. An apparatus as claimed in claim 19 wherein said counter includes circuitry for removing an integration contribution from said DC signal by deducting from said count value a deduction value corresponding to said integration contribution, thereby generating a reduced count value forming said integrated signal.

21. An apparatus as claimed in claim 14 further comprising an evaluation unit supplied with said integrated signal for evaluating said integrated signal to obtain information relating to said status of said sensor, said evaluating unit including a filter for filtering out unwanted information from said integrated signal.

22. An apparatus as claimed in claim 21 wherein said filter subjects said integrated signal to low-pass filtering to obtain a low-pass filtered signal, and wherein said evaluating unit includes a unit for evaluating said low-pass filtered signal to generate a value representing an orientation of said medical implant.

23. An apparatus as claimed in claim 22 wherein said unit for evaluating said low-pass filtered signal compares said low-pass filtered signal to respective, predetermined threshold values, said threshold values respectively corresponding to predetermined orientations of said medical implant, to obtain a comparison result as said value representing an orientation of the medical implant.

24. An apparatus as claimed in claim 21 further comprising an additional evaluating unit containing a bandpass filter for bandpass filtering said integrated signal to obtain a bandpass filtered signal, and a unit for evaluating said bandpass filtered signal to obtain a value representing a physical activity level of a person in whom said medical implant is implanted.

25. An apparatus as claimed in claim 14 wherein said sensor is sensitive to positive and negative changes in said load in only one direction.

26. An apparatus as claimed in claim 14 wherein said sensor is a piezoelectric sensor, and further